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10/046,333	10/26/2001	Michael S. Foster	030048026US	2814

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EXAMINER	
NGO, NGUYEN [illegible]	
ART UNIT	PAPER NUMBER
2663	

DATE MAILED: 01/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/046,333	FOSTER ET AL.	
	Examiner	Art Unit	
	Nguyen Ngo	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This communication is in response to the amendment of November 3, 2005. All changes made to the Specification, and Claims have been entered. Accordingly, Claims 1-57 are currently pending in the application.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 8, 9, 12-14, 16-18, 25, 26, 29-31, 33-36, 38, 39, 41-43, 45, 50, and 57 are rejected under 35 U.S.C. 102(e) as being anticipated by Anderson et al. (US 6597691), hereinafter referred to as Anderson.

Regarding claim 1, Anderson discloses a high performance switching topology and frame addressing technique (method in a routing device for identifying a destination port for data) comprising;

Fibre Channel switch modules referred to as chassis (col3 lines 18) with distinct Chassis Numbers identifying one of the possible chassis (domain address associated with the routing device, col5 lines 44-45). Anderson further discloses with figure 9B,

that the CN is used to differentiate between chassis (domains) and that a frame uses it's destination ID field, comprising a CN field and PN field, (D_ID which correlates to the domain address associated with the data) to compare to the CN of a specific module (comparing a domain address associated with the data (D_ID) with a domain address associated with the routing device (CN), col11 line 51-55). Examiner interprets the Chassis numbers to correlate to domain addresses, and it is further noted that Anderson discloses that each Chassis communicates with a loop of devices (routing devices use domain addresses (Chassis number) to forward data between domains (between Chassis), and wherein one domain address is assigned to routing devices in that domain (Chassis Number (domain address) representing the loop of devices), figure 2 and col3 lines 63-66) and that there is a CN value that represent distinct Chassis (col6 lines 16-18).

that if the D_ID chassis number is not equal to the CN of the receiving chassis, then the frame will have to be routed to a different chassis (col11 line53-55), and the E_Ports are used to access the other chassis (when the domain address associated with the data does not match the domain address associated with the routing device, identifying a port (E_Ports) based on the domain address associated with the data, col12 lines 1-3).

that if the D_ID chassis number is equal to the CN of the chassis, then routing will be completed (col11 lines 57-58) and the chassis will route the frame to the destination fabric port using the Port Number (PN) field which may be either F_Ports or FL_Ports (col6 lines 45-46). Anderson further discloses a virtual ID represents a port

number (when the domain address associated with the data matches the domain address associated with the routing device, identifying a port based on a virtual address associated with the data and wherein the identified port is the destination port for the data, col14 lines 28-30).

Regarding claim 8, Anderson discloses of parsing the D_ID (virtual identifier) in a manner that allows routing the frame through all of the topologies, more specifically into a PN field (virtual address) and a CN field (domain address) (wherein the domain address and virtual address of the data form a virtual identifier, col5 lines 29-45).

Regarding claim 9, Anderson discloses the preferred embodiments of the switching method are described in the Fibre Channel Standard (wherein the data is a Fibre Channel Frame, col3 lines 10-12).

Regarding claim 12, Anderson discloses that the chassis is a Fibre Channel Switch module (routing device is an interconnect fabric module, col3 lines 17-18).

Regarding claim 13, Anderson discloses each switch chassis has a switch for selectively transmitting data frames between selected ones of its ports (transmitting the data through the identified port).

Regarding claim 14, Anderson discloses the preferred embodiments of the switching method are described in the Fibre Channel Standard (the routing device is Fibre Channel compatible, col3 lines 10-12).

Regarding claim 16, Anderson discloses that if a frame is received on a fabric port in chassis 0, and the frame destination is in chassis 2, it will route the frame to a E_Port where the frame will be routed to the destination fabric port using the CN field to compare at the destination chassis (wherein a port identified using the domain address associated with the data is a port through which the data can be sent to a routing device with a domain address that matches the domain address of the data (in this case it is chassis 2, col6 lines 46-50).

Regarding claim 17, Anderson discloses that the chassis is a Fibre Channel Switch module (routing device is a switch, col3 lines 17-18).

Regarding claim 18, Anderson discloses a high performance switching topology and frame addressing technique (routing device) comprising;

a internal fabric controller located in each chassis, which includes a microprocessor that has a number of functions. The microprocessor, by talking to other microprocessors and other connected chassis can figure out the topology. Once it does that, it programs each chassis to tell them how to steer frames based on where they are in the topology (based on the CN and PN filed of the frame) (component that compares

the domain addresses and routes the frames based on the comparison and handles the method described below, col9 lines 37-47).

Fibre Channel switch modules referred to as chassis (col3 lines 18) with distinct Chassis Numbers identifying one of the possible chassis (domain address associated with the routing device, col5 lines 44-45). Anderson further discloses with figure 9B, that the CN is used to differentiate between chassis (domains) and that a frame uses it's destination ID field, comprising a CN field and PN field, (D_ID which correlates to the domain address associated with the data) to compare to the CN of a specific module (comparing a domain address associated with the data (D_ID) with a domain address associated with the routing device (CN), col11 line 51-55). Examiner interprets the Chassis numbers to correlate to domain addresses, and it is further noted that Anderson discloses that each Chassis communicates with a loop of devices (routing devices use domain addresses (Chassis number) to forward data between domains (between Chassis), and wherein one domain address is assigned to routing devices in that domain (Chassis Number (domain address) representing the loop of devices), figure 2 and col3 lines 63-66) and that there is a CN value that represent distinct Chassis (col6 lines 16-18).

that if the D_ID chassis number is not equal to the CN of the receiving chassis, then the frame will have to be routed to a different chassis (col11 line53-55), and the E_Ports are used to access the other chassis (when the domain address associated with the data does not match the domain address associated with the routing device,

identifying a port (E_Ports) based on the domain address associated with the data, col12 lines 1-3).

that if the D_ID chassis number is equal to the CN of the chassis, then routing will be completed (col11 lines 57-58) and the chassis will route the frame to the destination fabric port using the Port Number (PN) field which may be either F_Ports or FL_Ports (col6 lines 45-46). Anderson further discloses a virtual ID represents a port number (when the domain address associated with the data matches the domain address associated with the routing device, identifying a port based on a virtual address associated with the data and wherein the identified port is the destination port for the data, col14 lines 28-30).

Regarding claim 25, Anderson discloses of parsing the D_ID (virtual identifier) in a manner that allows routing the frame through all of the topologies, more specifically into a PN field (virtual address) and a CN field (domain address) (wherein the domain address and virtual address of the data form a virtual identifier, col5 lines 29-45).

Regarding claim 26, Anderson discloses the preferred embodiments of the switching method are described in the Fibre Channel Standard (wherein the data is a Fibre Channel Frame, col3 lines 10-12).

Regarding claim 29, Anderson discloses that the chassis is a Fibre Channel Switch module (routing device is an interconnect fabric module, col3 lines 17-18).

Regarding claim 30, Anderson discloses that the chassis is a Fibre Channel Switch module (routing device is a switch, col3 lines 17-18).

Regarding claim 31, Anderson discloses the preferred embodiments of the switching method are described in the Fibre Channel Standard (the routing device is Fibre Channel compatible, col3 lines 10-12).

Regarding claim 33, Anderson discloses that if a frame is received on a fabric port in chassis 0, and the frame destination is in chassis 2, it will route the frame to a E_Port where the frame will be routed to the destination fabric port using the CN field to compare at the destination chassis (wherein a port identified using the domain address associated with the data is a port through which the data can be sent to a routing device with a domain address that matches the domain address of the data (in this case it is chassis 2, col6 lines 46-50).

Regarding claim 34, Anderson discloses a data frame (storage medium) that parses the D_ID (virtual identifier) in a manner that allows routing the frame (storage medium containing a virtual identifier for communication, col5 lines 29-31). Anderson further discloses that the D_ID comprises;

a port number (PN) field, where a virtual ID represents a port number (a virtual address col9 line39-42).

a chassis number (CN) field (a domain address).

that if the D_ID chassis number is not equal to the CN of the receiving chassis, then the frame will have to be routed to a different chassis (col11 line53-55), and the E_Ports are used to access the other chassis (wherein the domain address is used to route the communication when a routing device has a domain address that does not match the domain address of the virtual identifier, col12 lines 1-3).

that if the D_ID chassis number is equal to the CN of the chassis, then routing will be completed (col11 lines 57-58) and the chassis will route the frame to the destination fabric port using the Port Number (PN) field which may be either F_Ports or FL_Ports (col6 lines 45-46). Anderson further discloses a virtual ID represents a port number (wherein the virtual address is used to route the communication when the routing device does not have a domain address that matches the domain address of the virtual identifier, col14 lines 28-30). Examiner interprets the Chassis numbers to correlate to domain addresses, and it is further noted that Anderson discloses that each Chassis communicates with a loop of devices (routing devices use domain addresses (Chassis number) to forward data between domains (between Chassis), and wherein one domain address is assigned to routing devices in that domain (Chassis Number (domain address) representing the loop of devices), figure 2 and col3 lines 63-66) and that there is a CN value that represent distinct Chassis (col6 lines 16-18).

Regarding claim 35, Anderson discloses that the data frame originates in one use chassis and travels to a destination in a different user chassis (storage medium is a data transmission medium, col4 lines 39-40).

Regarding claim 36, Anderson discloses a data frame (storage medium) that parses the D_ID or destination ID (virtual identifier) in a manner that allows routing the frame (virtual identifier is a destination identifier, col5 lines 29-31).

Regarding claim 38, Anderson discloses a data frame (storage medium) that parses the D_ID or destination ID (virtual identifier) in a manner that allows routing the frame (virtual identifier is part of a frame, col5 lines 29-31).

Regarding claim 39, Anderson discloses the preferred embodiments of the switching method are described in the Fibre Channel Standard (the frame is Fibre Channel compatible, col3 lines 10-12).

Regarding claim 41, Anderson discloses a method for data handling for switches and devices for use in data handling environments (method in a network of routing devices for routing communications). Anderson further discloses;

a data frame that parses the D_ID (virtual identifier) in a manner that allows routing the frame and that the D_ID comprises a port number (PN) field, where a virtual ID represents a port number (a virtual address col9 line39-42) and a chassis number

(CN, domain address) field (communication having a virtual identifier with a domain address and a virtual address that identifies a destination, col5 lines 29-31).

that if the D_ID chassis number is not equal to the CN of the receiving chassis, then the frame will have to be routed to a different chassis (col11 line53-55), and the E_Ports are used to access the other chassis (routing the received communication to the destination in accordance with the domain address when the domain address of the received communications does not match the domain address of a routing device, col12 lines 1-3).

that if the D_ID chassis number is equal to the CN of the chassis, then routing will be completed (col11 lines 57-58) and the chassis will route the frame to the destination fabric port using the Port Number (PN) field which may be either F_Ports or FL_Ports (col6 lines 45-46). Anderson further discloses a virtual ID represents a port number (routing the received communication to the destination in accordance with the virtual address when the domain address of the received communication does not match the domain address of a routing device, col14 lines 28-30). Examiner interprets the Chassis numbers to correlate to domain addresses, and it is further noted that Anderson discloses that each Chassis communicates with a loop of devices (routing devices use domain addresses (Chassis number) to forward data between domains (between Chassis), and wherein one domain address is assigned to routing devices in that domain (Chassis Number (domain address) representing the loop of devices), figure 2 and col3 lines 63-66) and that there is a CN value that represent distinct Chassis (col6 lines 16-18).

Regarding claim 42, Anderson discloses that the microprocessor has given specific chassis a chassis number (CN) as seen in figure 9A. The chassis on the left given a CN= 0, in the middle given a chassis of CN= 1, and chassis on the right given a CN= 2 (col11 lines 33-35) and further discloses that the switching network is built up from four separate networks or quadrants (col7 lines 3-5) and that a frame can be routed to the correct quadrant, and from there to the correct port (wherein the network comprises a collection of routing devices (chassis), each routing device being assigned to a domain with a domain address (CN depending on quadrant), col10 lines 42-45).

Regarding claim 43, Anderson discloses the preferred embodiments of the switching method are described in the Fibre Channel Standard (wherein the network is a Fibre Channel network, col3 lines 10-12).

Regarding claim 45, Anderson discloses that the chassis is a Fibre Channel Switch module (routing device is an interconnect fabric module, col3 lines 17-18).

Regarding claim 50, Anderson discloses a high performance switching topology and frame addressing technique (routing device) comprising;

Fibre Channel switch modules referred to as chassis (routing device, col3 lines 18) with distinct Chassis Numbers identifying one of the possible chassis (domain address associated with the routing device, col5 lines 44-45). Anderson further

discloses with figure 9B, that the CN is used to differentiate between chassis (domains) and that a frame uses it's destination ID field, comprising a CN field and PN field, (D_ID which correlates to the domain address associated with the data) to compare to the CN of a specific module (col11 line 51-55) and that if the D_ID chassis number is not equal to the CN of the receiving chassis, then the frame will have to be routed to a different chassis (col11 line53-55), and the E_Ports are used to access the other chassis (means for identifying a port based on a domain address associated with a communication when the domain address associated with the communication does not match a domain address associated with the routing device, col12 lines 1-3).

that if the D_ID chassis number is equal to the CN of the chassis, then routing will be completed (col11 lines 57-58) and the chassis will route the frame to the destination fabric port using the Port Number (PN) field which may be either F_Ports or FL_Ports (col6 lines 45-46). Anderson further discloses a virtual ID represents a port number (means for identifying a port based on a virtual address associated with the communication when the domain address associated with the communication matches the domain address associated with the routing device and means for forwarding the communication via the identified port, col14 lines 28-30).

Regarding claim 57, Anderson discloses of parsing the D_ID (virtual identifier) in a manner that allows routing the frame through all of the topologies, more specifically into a PN field (virtual address) and a CN field (domain address) (wherein the domain address and virtual address of the data form a virtual identifier, col5 lines 29-45).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 2, 3, 4, 5, 6, 7, 11, 19, 20, 21, 22, 23, 24, 28, 46, 47, 48, 49, 51, 52, 53, 54, 55 and 56 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson et al. (US 6597691) in view of Tasaki et al. (US 6895006), hereinafter referred to as Anderson and Tasaki.

Regarding claim 2, Anderson fails to disclose the specific limitations of claim 2, using the domain address to index a domain address table to retrieve an identification of the port. Anderson however discloses that a microprocessor for handling the chassis (including identifying specific ports) includes the usual supporting subsystems such as static RAM, flash RAM, and PROM memory and that the microprocessor is the heart of the internal fabric controller (col7 lines 21-28). This thus provides the motivation to use

the memory as stated above, to identify any specific port for forwarding frames in an efficient manner.

Tasaki discloses of an internal cell receiving section that has a function to extract a header field from the cell (frame) and uses an index search section to get output port information (identification of the specific port) corresponding to the output index information included in the header field (domain address corresponding to output index information included in the header field) by referring to an output conversion table (using the domain address to index a domain address table to retrieve an identification of the port, col2 lines 45-50). Tasaki further discloses that when an output port conversion table is used, memory such as RAM or ROM is used as stated in Anderson (col3 lines 55-57).

It should thus be obvious to a person skilled in the art to incorporate the output conversion table disclosed by Tasaki into the frame addressing technique, more specifically the microprocessor which includes RAM for managing the Fiber Channel switch disclosed by Anderson to efficiently and effectively identify the a specific output port for forwarding a data frame in a switch.

Regarding claim 3, Anderson and Tasaki disclose all the limitation of claim 3. More specifically, Tasaki discloses that the output port conversion table is a table to store multiple index information and multiple output port number information in the form of

one to one or one to multiple (each entry of the domain address table contains a port map that designates one or more of the ports of the routing device, col2 lines 48-50).

Regarding claim 4, Anderson and Tasaki disclose all the limitations of claim 4 as discussed with claim 2. More specifically Tasaki discloses of using an index search section to get output port information (identification of the specific port) corresponding to the output index information included in the header field by referring to an output conversion table (col2 lines 45-50), where the table stores multiple index information and multiple output port number information in the form of one to one or one to multiple (identifies each of the ports designated by a retrieved port map, col2 lines 48-50).

Regarding claim 5, Anderson fails to disclose the specific limitations of claim 5, using the virtual address to index a virtual address table to retrieve an identification of the port. Anderson however discloses that a microprocessor for handling the chassis (including identifying specific ports) includes the usual supporting subsystems such as static RAM, flash RAM, and PROM memory and that the microprocessor is the heart of the internal fabric controller (col7 lines 21-28). This thus provides the motivation to use the memory as stated above, to identify any specific port for forwarding frames in an efficient manner.

Tasaki discloses of an internal cell receiving section that has a function to extract a header field from the cell (frame) and uses an index search section to get output port

information (identification of the specific port) corresponding to the output index information included in the header field (virtual address corresponding to output index information included in the header field) by referring to an output conversion table (using the virtual address to index a virtual address table to retrieve an identification of the port, col2 lines 45-50). Tasaki further discloses that when an output port conversion table is used, memory such as RAM or ROM is used as stated in Anderson (col3 lines 55-57).

It should thus be obvious to a person skilled in the art to incorporate the output conversion table disclosed by Tasaki into the frame addressing technique, more specifically the microprocessor which includes RAM for managing the Fiber Channel switch disclosed by Anderson to efficiently and effectively identify the a specific output port for forwarding a data frame in a switch.

Regarding claim 6, Anderson and Tasaki disclose all the limitation of claim 6. More specifically, Tasaki discloses that the output port conversion table is a table to store multiple index information and multiple output port number information in the form of one to one or one to multiple (each entry of the virtual address table contains a port map that designates one or more of the ports of the routing device, col2 lines 48-50).

Regarding claim 7, Anderson and Tasaki disclose all the limitations of claim 7 as discussed with claim 5. More specifically Tasaki discloses of using an index search

section to get output port information (identification of the specific port) corresponding to the output index information included in the header field by referring to an output conversion table (col2 lines 45-50), where the table stores multiple index information and multiple output port number information in the form of one to one or one to multiple (identifies each of the ports designated by a retrieved port map, col2 lines 48-50).

Regarding claim 11, Anderson fails to disclose the specific limitations of claim 11, each port has its own virtual address table and the table of the port is used to identify the port. Anderson however discloses that a microprocessor for handling the chassis (including identifying specific ports) includes the usual supporting subsystems such as static RAM, flash RAM, and PROM memory and that the microprocessor is the heart of the internal fabric controller (col7 lines 21-28). This thus provides the motivation to use the memory as stated above, to identify any specific port for forwarding frames in an efficient manner.

Tasaki discloses of an internal cell receiving section (which should be obvious to be located in each port) that has a function to extract a header field from the cell (frame) and uses an index search section to get output port information (identification of the specific port) corresponding to the output index information included in the header field by referring to an output conversion table (virtual address table of the port through which the data is received is used to identify the port, col2 lines 45-50). Tasaki further

discloses that when an output port conversion table is used, memory such as RAM or ROM is used as stated in Anderson (col3 lines 55-57).

It should thus be obvious to a person skilled in the art to incorporate the output conversion table disclosed by Tasaki into the frame addressing technique, more specifically the microprocessor which includes RAM for managing the Fiber Channel switch disclosed by Anderson to efficiently and effectively identify the a specific output port for forwarding a data frame in a switch. It should further be obvious that the each port of the switch has its own output port conversion table (has its own virtual address table).

Regarding claim 19, Anderson fails to disclose the specific limitations of claim 19, of having a domain address table that uses the domain address to retrieve an identification of the port from the domain address table. Anderson however discloses that a microprocessor for handling the chassis (including identifying specific ports) includes the usual supporting subsystems such as static RAM, flash RAM, and PROM memory and that the microprocessor is the heart of the internal fabric controller (col7 lines 21-28). This thus provides the motivation to use the memory as stated above, to identify any specific port for forwarding frames in an efficient manner.

Tasaki discloses of an internal cell receiving section that has a function to extract a header field from the cell (frame) and uses an index search section to get output port

information (identification of the specific port) corresponding to the output index information included in the header field by referring to an output conversion table (including a domain address table with a mapping of domain addresses to destination ports, and uses the domain address to retrieve an identification of the port from the domain address table, col2 lines 45-50). Tasaki further discloses that when an output port conversion table is used, memory such as RAM or ROM is used as stated in Anderson (col3 lines 55-57).

It should thus be obvious to a person skilled in the art to incorporate the output conversion table disclosed by Tasaki into the frame addressing technique, more specifically the microprocessor which includes RAM for managing the Fiber Channel switch disclosed by Anderson to efficiently and effectively identify the a specific output port for forwarding a data frame in a switch.

Regarding claim 20, Anderson and Tasaki disclose all the limitation of claim 20. More specifically, Tasaki discloses that the output port conversion table is a table to store multiple index information and multiple output port number information in the form of one to one or one to multiple (each entry of the domain address table contains a port map that designates one or more of the ports of the routing device, col2 lines 48-50).

Regarding claim 21, Anderson and Tasaki disclose all the limitations of claim 21 as discussed with claim 19. More specifically Tasaki discloses of using an index search

section to get output port information (identification of the specific port) corresponding to the output index information included in the header field by referring to an output conversion table (col2 lines 45-50), where the table stores multiple index information and multiple output port number information in the form of one to one or one to multiple (identifies each of the ports designated by a retrieved port map, col2 lines 48-50).

Regarding claim 22, Anderson fails to disclose the specific limitations of claim 22, of having a virtual address table that uses the virtual address to retrieve an identification of the port from the virtual address table. Anderson however discloses that a microprocessor for handling the chassis (including identifying specific ports) includes the usual supporting subsystems such as static RAM, flash RAM, and PROM memory and that the microprocessor is the heart of the internal fabric controller (col7 lines 21-28). This thus provides the motivation to use the memory as stated above, to identify any specific port for forwarding frames in an efficient manner.

Tasaki discloses of an internal cell receiving section that has a function to extract a header field from the cell (frame) and uses an index search section to get output port information (identification of the specific port) corresponding to the output index information included in the header field by referring to an output conversion table (including a virtual address table with a mapping of virtual addresses to destination ports, and uses the virtual address to retrieve an identification of the port from the virtual address table, col2 lines 45-50). Tasaki further discloses that when an output port

conversion table is used, memory such as RAM or ROM is used as stated in Anderson (col3 lines 55-57).

It should thus be obvious to a person skilled in the art to incorporate the output conversion table disclosed by Tasaki into the frame addressing technique, more specifically the microprocessor which includes RAM for managing the Fiber Channel switch disclosed by Anderson to efficiently and effectively identify the a specific output port for forwarding a data frame in a switch.

Regarding claim 23, Anderson and Tasaki disclose all the limitation of claim 23. More specifically, Tasaki discloses that the output port conversion table is a table to store multiple index information and multiple output port number information in the form of one to one or one to multiple (each entry of the virtual address table contains a port map that designates one or more of the ports of the routing device, col2 lines 48-50).

Regarding claim 24, Anderson and Tasaki disclose all the limitations of claim 24 as discussed with claim 22. More specifically Tasaki discloses of using an index search section to get output port information (identification of the specific port) corresponding to the output index information included in the header field by referring to an output conversion table (col2 lines 45-50), where the table stores multiple index information

and multiple output port number information in the form of one to one or one to multiple (identifies each of the ports designated by a retrieved port map, col2 lines 48-50).

Regarding claim 28, Anderson fails to disclose the specific limitations of claim 28, each port has its own virtual address table and the table of the port is used to identify the port. Anderson however discloses that a microprocessor for handling the chassis (including identifying specific ports) includes the usual supporting subsystems such as static RAM, flash RAM, and PROM memory and that the microprocessor is the heart of the internal fabric controller (col7 lines 21-28). This thus provides the motivation to use the memory as stated above, to identify any specific port for forwarding frames in an efficient manner.

Tasaki discloses of an internal cell receiving section (which should be obvious to be located in each port) that has a function to extract a header field from the cell (frame) and uses an index search section to get output port information (identification of the specific port) corresponding to the output index information included in the header field by referring to an output conversion table (virtual address table of the port through which the data is received is used to identify the port, col2 lines 45-50). Tasaki further discloses that when an output port conversion table is used, memory such as RAM or ROM is used as stated in Anderson (col3 lines 55-57).

It should thus be obvious to a person skilled in the art to incorporate the output conversion table disclosed by Tasaki into the frame addressing technique, more specifically the microprocessor which includes RAM for managing the Fiber Channel switch disclosed by Anderson to efficiently and effectively identify the a specific output port for forwarding a data frame in a switch. It should further be obvious that the each port of the switch has its own output port conversion table (has its own virtual address table).

Regarding claim 46, Anderson fails to disclose the specific limitations of claim 46,has a domain address table that maps domain addresses to ports of the routing device. Anderson however discloses that a microprocessor for handling the chassis (including identifying specific ports) includes the usual supporting subsystems such as static RAM, flash RAM, and PROM memory and that the microprocessor is the heart of the internal fabric controller (col7 lines 21-28). This thus provides the motivation to use the memory as stated above, to identify any specific port for forwarding frames in an efficient manner.

Tasaki discloses of an internal cell receiving section that has a function to extract a header field from the cell (frame) and uses an index search section to get output port information (identification of the specific port) corresponding to the output index information included in the header field by referring to an output conversion table (maps domain addresses to ports of the routing devicecol2 lines 45-50). Tasaki further

discloses that when an output port conversion table is used, memory such as RAM or ROM is used as stated in Anderson (col3 lines 55-57).

It should thus be obvious to a person skilled in the art to incorporate the output conversion table disclosed by Tasaki into the frame addressing technique, more specifically the microprocessor which includes RAM for managing the Fiber Channel switch disclosed by Anderson to efficiently and effectively identify the a specific output port for forwarding a data frame in a switch.

Regarding claim 47, Anderson and Tasaki disclose al the limitation of claim 47, more specifically Tasaki discloses of an internal cell receiving section that has a function to extract a header field from the cell (frame). It should be obvious to have this receiving cell section and the output conversion table for each specific port of the switch (each port has its own domain address table).

Regarding claim 48, Anderson fails to disclose the specific limitations of claim 48, has a virtual address table that maps domain addresses to ports of the routing device. Anderson however discloses that a microprocessor for handling the chassis (including identifying specific ports) includes the usual supporting subsystems such as static RAM, flash RAM, and PROM memory and that the microprocessor is the heart of the internal fabric controller (col7 lines 21-28). This thus provides the motivation to use the memory

as stated above, to identify any specific port for forwarding frames in an efficient manner.

Tasaki discloses of an internal cell receiving section that has a function to extract a header field from the cell (frame) and uses an index search section to get output port information (identification of the specific port) corresponding to the output index information included in the header field by referring to an output conversion table (maps virtual addresses to ports of the routing device, col2 lines 45-50). Tasaki further discloses that when an output port conversion table is used, memory such as RAM or ROM is used as stated in Anderson (col3 lines 55-57).

It should thus be obvious to a person skilled in the art to incorporate the output conversion table disclosed by Tasaki into the frame addressing technique, more specifically the microprocessor which includes RAM for managing the Fiber Channel switch disclosed by Anderson to efficiently and effectively identify the a specific output port for forwarding a data frame in a switch.

Regarding claim 49, Anderson and Tasaki disclose al the limitation of claim 49, more specifically Tasaki discloses of an internal cell receiving section that has a function to extract a header field from the cell (frame). It should be obvious to have this receiving cell section and the output conversion table for each specific port of the switch (each port has its own virtual address table).

Regarding claim 51, Anderson fails to disclose the specific limitations of claim 51, uses the domain address to retrieve an identification of the port from mapping. Anderson however discloses that a microprocessor for handling the chassis (including identifying specific ports) includes the usual supporting subsystems such as static RAM, flash RAM, and PROM memory and that the microprocessor is the heart of the internal fabric controller (col7 lines 21-28). This thus provides the motivation to use the memory as stated above, to identify any specific port for forwarding frames in an efficient manner.

Tasaki discloses of an internal cell receiving section that has a function to extract a header field from the cell (frame) and uses an index search section to get output port information (identification of the specific port) corresponding to the output index information included in the header field by referring to an output conversion table (uses the domain address to retrieve an identification of the port from the mapping (output port table), col2 lines 45-50). Tasaki further discloses that when an output port conversion table is used, memory such as RAM or ROM is used as stated in Anderson (col3 lines 55-57).

It should thus be obvious to a person skilled in the art to incorporate the output conversion table disclosed by Tasaki into the frame addressing technique, more specifically the microprocessor which includes RAM for managing the Fiber Channel

switch disclosed by Anderson to efficiently and effectively identify the a specific output port for forwarding a data frame in a switch.

Regarding claim 52, Anderson and Tasaki disclose all the limitation of claim 52. More specifically, Tasaki discloses that the output port conversion table is a table to store multiple index information and multiple output port number information in the form of one to one or one to multiple (each mapping includes a port map that designates one ore more of the ports of the routing device, col2 lines 48-50).

Regarding claim 53, Anderson and Tasaki disclose all the limitations of claim 53 as discussed with claim 51. More specifically Tasaki discloses of using an index search section to get output port information (identification of the specific port) corresponding to the output index information included in the header field by referring to an output conversion table (col2 lines 45-50), where the table stores multiple index information and multiple output port number information in the form of one to one or one to multiple (identifies each of the ports designated by a retrieved port map, col2 lines 48-50).

Regarding claim 54, Anderson fails to disclose the specific limitations of claim 54, uses the virtual address to retrieve an identification of the port from mapping. Anderson however discloses that a microprocessor for handling the chassis (including identifying specific ports) includes the usual supporting subsystems such as static RAM, flash RAM, and PROM memory and that the microprocessor is the heart of the internal fabric

controller (col7 lines 21-28). This thus provides the motivation to use the memory as stated above, to identify any specific port for forwarding frames in an efficient manner.

Tasaki discloses of an internal cell receiving section that has a function to extract a header field from the cell (frame) and uses an index search section to get output port information (identification of the specific port) corresponding to the output index information included in the header field by referring to an output conversion table (uses the virtual address to retrieve an identification of the port from the mapping (output port table), col2 lines 45-50). Tasaki further discloses that when an output port conversion table is used, memory such as RAM or ROM is used as stated in Anderson (col3 lines 55-57).

It should thus be obvious to a person skilled in the art to incorporate the output conversion table disclosed by Tasaki into the frame addressing technique, more specifically the microprocessor which includes RAM for managing the Fiber Channel switch disclosed by Anderson to efficiently and effectively identify the a specific output port for forwarding a data frame in a switch.

Regarding claim 55, Anderson and Tasaki disclose all the limitation of claim 55. More specifically, Tasaki discloses that the output port conversion table is a table to store multiple index information and multiple output port number information in the form of

one to one or one to multiple (each mapping includes a port map that designates one ore more of the ports of the routing device, col2 lines 48-50).

Regarding claim 56, Anderson and Tasaki disclose all the limitations of claim 56 as discussed with claim 54. More specifically Tasaki discloses of using an index search section to get output port information (identification of the specific port) corresponding to the output index information included in the header field by referring to an output conversion table (col2 lines 45-50), where the table stores multiple index information and multiple output port number information in the form of one to one or one to multiple (identifies each of the ports designated by a retrieved port map, col2 lines 48-50).

8. Claims 10, 15, 27, 32, 37, 40, and 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson et al. (US 6597691), hereinafter referred to as Anderson

Regarding claim 10, Anderson fails to disclose that the data is an InfiniBand Channel frame. It is well known in the art that data can be transmitted through the interconnect fabric as frames such as those defined by the Fibre Channel and the InfiniBand standards. It should thus be obvious to a person skilled in the art that the data can be an InfiniBand Channel instead of a Fibre Channel frame.

Regarding claim 15, Anderson fails to disclose that the routing device is InfiniBand compatible. It is well known in the art that data can be transmitted through the

interconnect fabric as frames such as those defined by the Fibre Channel and the InfiniBand standards. It should thus be obvious to a person skilled in the art that the routing device is InfiniBand compatible.

Regarding claim 27, Anderson fails to disclose that the data is an InfiniBand Channel frame. It is well known in the art that data can be transmitted through the interconnect fabric as frames such as those defined by the Fibre Channel and the InfiniBand standards. It should thus be obvious to a person skilled in the art that the data can be an InfiniBand Channel instead of a Fibre Channel frame.

Regarding claim 32, Anderson fails to disclose that the routing device is InfiniBand compatible. It is well known in the art that data can be transmitted through the interconnect fabric as frames such as those defined by the Fibre Channel and the InfiniBand standards. It should thus be obvious to a person skilled in the art that the routing device is InfiniBand compatible.

Regarding claim 37, Anderson discloses that the Fibre Channel Source ID field is utilized. It should thus be obvious that the virtual identifier may be a source identifier containing the CN and PN fields instead of the destination identifier mentioned above.

Regarding claim 27, Anderson fails to disclose that the data is an InfiniBand Channel frame. It is well known in the art that data can be transmitted through the interconnect fabric as frames such as those defined by the Fibre Channel and the InfiniBand

standards. It should thus be obvious to a person skilled in the art that the data can be an InfiniBand Channel instead of a Fibre Channel frame.

Regarding claim 44, Anderson fails to disclose that the network is an InfiniBand network. It is well known in the art that data can be transmitted through the interconnect fabric as frames such as those defined by the Fibre Channel and the InfiniBand standards. It should thus be obvious to a person skilled in the art that the network can be an InfiniBand network instead of a Fibre Channel network.

Response to Arguments

6. Applicant's arguments filed November 03,2005 have been fully considered but they are not persuasive.

7. The applicant submits that Anderson does not teach the limitation that if a domain address associated with a frame that is received by a routing device does not match the domain address associated with the routing device then the frame will be routed to its proper destination domain using the domain address associated with the frame. Applicant further argues that "CN" (Chassis Number) may not be represented as "domain address", and that Anderson does not use CN to send anything from one domain of multiple devices to another domain of multiple devices. Examiner posits that it is not unreasonable to interpret the CN disclosed by Anderson as a domain address, as it serves as an identification of different Chassis (different domains) further representing a loop of devices (figure 2 and col3 lines 60-67). CN identifies a single

chassis, which represents a loop of devices (domain of multiple devices). It is further seen from George (US 6,697,359), High Performance Switch Fabric Element and Switch System, that a single chassis represent a Domain (col3 lines 26-28 and col9 lines 4-6). George further discloses that different Chassis will have different Domain numbers (CN) and that if the destination Domain is the same as the input port Domain, the frame stays on the chassis; if different, it is routed to another chassis containing a loop of devices (another domain of multiple devices, col11 lines 9-30)). It is thus apparent that the CN as disclosed from Anderson correlate to a domain address as seen from George.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) George (U.S 6697359) High Performance Switch Fabric Element and Switch Systems.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nguyen Ngo whose telephone number is (571)272-8398. The examiner can normally be reached on Monday-Friday 7am - 3:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571)272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N.N.

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RICKY Q. NGO
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